WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a plurality of word lines;

a plurality of bit lines; and

a plurality of static memory cells each having a first, second, third, fourth, fifth, and sixth transistors,

wherein each of channels of said first, second, third, and fourth transistors are formed vertical against a substrate of the semiconductor memory device.

2. The memory device according to claim 1, wherein each of semiconductor regions forming a source or a drain of said fifth and sixth transistors forms a PN junction against said substrate.

3. The memory device according to claim 2,

wherein gate electrodes of said fifth and sixth transistors are coupled to said word lines, and

wherein each source-drain path of said fifth and sixth transistors are coupled to said bit lines.

4. The memory device according to claim 2,

wherein a gate electrode of said fifth transistor is coupled to the drain of said sixth transistor,

wherein a gate electrode of said sixth transistor is coupled to the drain of said fifth transistor, and

wherein each of said fifth and sixth transistors has the same conductivity type as said first and second transistors.

5. The semiconductor memory device according to claim 2,

wherein a gate electrode of said fifth transistor is coupled to the drain of said sixth transistor,

wherein a gate electrode of said sixth transistor is coupled to the drain of said fifth transistor, and

wherein each of said fifth and sixth transistors has a different conductivity type from said first and second transistors.

6. The semiconductor memory device according to claim 1,

wherein gate electrodes of the first and second transistors are formed on a first layer, and

wherein gate electrodes of the third and fourth transistors are formed on a second layer.

7. The semiconductor memory device according to claim 1,

wherein a gate electrode of the first transistor is formed on a first layer,

wherein a gate electrode of the second transistor is formed on a second layer,

wherein a gate electrode of the third transistor is formed on a third layer, and

wherein a gate electrode of the fourth transistor is formed on a fourth layer.

8. The semiconductor memory device according to claim 1,

wherein a column forming the channel of the first transistor is covered with a gate electrode surrounding a cylindrical surface of the column with an insulating layer therebetween.

9. The semiconductor memory device according to claim 1,

wherein the channels of said fifth, and sixth transistor are formed vertical against the substrate, and wherein said substrate is made of single crystal silicon.

10. A SRAM device having a plurality of SRAM cells, at least one of which is a vertical SRAM cell comprising at least four vertical transistors onto a substrate, wherein each vertical transistor includes a source, a drain, and a channel therebetween aligning in one aligning line which penetrates into the substrate surface at an angle greater than zero degree.

11. The SRAM device according to claim 10, wherein the angle is 90 degree.

12. The SRAM device according to claim 10, wherein the vertical SRAM cell further comprising a pair of resistors, a pair of horizontal transistors, or an additional pair of vertical transistors.

13. The SRAM device according to claim 12, wherein the pair horizontal transistors or the additional pair of vertical transistors operate as a pair of transfer, drive, or load MOS transistors, and wherein the load transistors are PMOS transistors while the transfer and driver transistors are NMOS transistors.

14. The SRAM device according to claim 12, wherein the four vertical transistors are divided into two groups located in two different levels, and the vertical SRAM cell further comprises the pair of resistors or the additional pair of vertical transistors, either pair is arranged in one of the two levels, or above, below, or in between the two levels.

15. The SRAM device according to claim 14, wherein the transistors or resistors located in different levels are selectively connected to each other via at least one vertical interconnect which is parallel with said aligning line.

16. The SRAM device according to claim 15, wherein said at least one vertical interconnect cross links with at least one of a horizontal interconnect, a horizontal Vcc beam, and a horizontal Vss beam, each of which is parallel with the substrate surface.

17. The SRAM device according to claim 15, wherein said at least one vertical interconnect penetrates through at least one gate electrode of the vertical transistor with a first dimension and a second dimension parallel with the substrate surface, and a third dimension parallel with said aligning line.

18. The SRAM device according to claim 17, wherein said at least one vertical interconnect penetrates through at least two of said gate electrodes.

19. The SRAM device according to claim 15, wherein said at least one vertical interconnect include two vertical interconnects connecting with two vertical transistors respectively thereby forming one unit SRAM cell thereamong in a shape of a diagonal or parallelogram on a cross section parallel with the substrate surface.

20. The SRAM device according to claim 12, wherein the vertical SRAM cell further comprising at least one pair bit lines being respectively connected to at least one of the transistors and resistors via two vertical interconnects which are parallel with said aligning line, and each of the bit lines is connected with a plurality of bit line contacts, each of which is shared by two adjacent SRAM cells of the plurality of SRAM cells.

21. The SRAM device according to claim 12, wherein said each vertical transistor further includes a gate electrode with a first dimension and a second dimension parallel with the substrate surface, and a third dimension parallel with said aligning line.

22. The SRAM device according to claim 10, further comprising at least another vertical SRAM cell built above the vertical SRAM cell with a dielectric layer therebetween.